工業技術研究院
Industrial Technology Research Institute

財物_採購規範書
(自駕控制器運算模組)

✧ **目的/用途說明：**

■ 目的/用途：執行經濟部107年度自動駕駛中型巴士開發計畫，搭配硬體系統介面整合及軟體應用及控制程式用自駕控制器運算模組。

✧ **規格/功能需求：**

■ 需求規格、數量/外觀尺寸：

(1) 自駕控制器運算模組1, 數量1具

(2) 自駕控制器運算模組2, 數量1具

■ 相關圖說規格文件

(1) 自駕控制器運算模組 1 規格

Item	Specification
2x Xavier SoC with integrate Hardware Engines	◦8-core "Carmel" CPUs based on ARM v8 ISA ◦Deep Learning Accelerator (DLA): 5 TOPS (FP16) | 10 TOPS (INT8) ◦Volta-class GPU: 20 TOPS (INT8) | 1.3 TFLOPS (FP32) ◦Programmable Vision Accelerator (PVA): 1.6 TOPS ◦Stereo and Optical Flow Engine (SOFE): 6 TOPS ◦Image Signal Processor (ISP): 1.5 Giga Pixels/s ◦Video Encoder: 1.2 GPix/s ◦Video Decoder: 1.8 GPix/s
2x "Turing" Discrete GPU	◦Discrete GPU: 130 TOPS connected to Xavier SoC over NVLink (20GB/s)
System I/O	◦Camera: >90 Gb/s over 16x GMSL(R) ports ◦Lidar/Radar: ~50 Gb/s over Ethernet ◦Vehicle IO: 16 CAN interfaces
Memory Bandwidth	◦Xavier: >250 GB/s ◦Discrete GPU: > 750 GB/s ◦Overall: >1 TB/s

(2) 自駕控制器運算模組2規格

Item	Specification
1x Xavier SoC with integrate Hardware Engines	◦8-core "Carmel" CPUs based on ARM v8 ISA ◦Deep Learning Accelerator (DLA): 5 TOPS (FP16) | 10 TOPS (INT8) ◦Volta-class GPU: 20 TOPS (INT8) | 1.3 TFLOPS (FP32) ◦Programmable Vision Accelerator (PVA): 1.6 TOPS ◦Stereo and Optical Flow Engine (SOFE): 6 TOPS ◦Image Signal Processor (ISP): 1.5 Giga Pixels/s ◦Video Encoder: 1.2 GPix/s ◦Video Decoder: 1.8 GPix/s
System I/O	◦Camera: >90 Gb/s over 16x GMSL(R) ports ◦Lidar/Radar: ~50 Gb/s over Ethernet ◦Vehicle IO: 16 CAN interfaces
Memory	◦Xavier: >250 GB/s

Bandwidth	◦Discrete GPU: > 750 GB/s ◦Overall: >1 TB/s

✧ **安裝/測試要求：無**

✧ **檢測/驗收標準：**
依照規格測試驗收

✧ **交貨期：107年 12月 25日前**

✧ **保固：** 驗收合格後提供免費保固12個月